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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,556	03/12/2001	Jaroslav Hynecek	ISE103	9129

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EXAMINER	
YODER III, CHRISS S	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,556	HYNECEK, JAROSLAV	
	Examiner	Art Unit	
	Chriss S. Yoder, III	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7-10, and 12* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2 and 12 are objected to because of the following informalities:

Claim 2 recites the limitation "each *charge conversion* node" in line 4 of claim 2, which the examiner believes should read "each *detection* node."

Claim 12 is misnumbered. The examiner believes that claim 12 should be renumbered 11.

These claims will be examined as understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaplan (US Patent # 5,867,215).

3. In regard to claim 1, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture that incorporates charge multipliers (24), said image sensor including a first CCD register (14) adjacent to at least a second CCD register (16) and coupled to the said first register through a charge overflow barrier (22).

4. In regard to claim 2, note Kaplan discloses the use of that the second adjacent CCD register collects overflow charge (column 4, lines 33-39; the overflow charge is sent to the second CCD register, 16) and transports it to at least one detection node

located in each register (column 4, lines 40-51; the transport of the signal from the CCD well to the amplifier is considered to be the equivalent of the detection node), and each detection node having charge conversion sensitivity that may be different for each node (column 5, lines 1-6; although not explicitly stated, it is inherent that the sensitivity changes with respect to the charge handling capabilities, and the CCD registers, 14 and 16, are of different charge handling capabilities).

5. In regard to claim 3, note Kaplan discloses that the signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula (column 5, lines 45-61).

6. In regard to claim 9, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture, said readout architecture incorporating charge multipliers (24 and 26), CCD registers (14 and 16), and a charge overflow device in at least one of its registers (22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (US Patent # 6,444,968) in view of Farrier et al. (US Patent # 6,392,260).

8. In regard to claim 4, note Burt discloses the use of a solid-state image sensor (2) having a readout architecture that incorporates charge multipliers (column 4, lines 55-

64; and figure 1: 5 and 10), said image sensor including: a CCD register that incorporates at least one charge-multiplication device element in at least one stage (column 4, lines 55-64; and figure 1: 5 and 10). Therefore, it can be seen that the Burt device lacks the use of said at least one stage having a progressively wider width. Farrier discloses the use of a CCD register having a progressively wider width (column 7, line 66 – column 8, line 28; and figure 3: 110). Farrier teaches that the use of a progressively wider width is preferred in order to carry all the charge transferred without blooming (column 8, lines 25-28). Therefore, it would have been obvious to one of ordinary skill in the art to modify the Burt device to include the use of a progressively wider width as suggested by Farrier.

9. In regard to claim 8, note Burt discloses that the CCD register has a charge overflow barrier (16) and a charge overflow drain (17) incorporated in at least one of its stages to prevent charge blooming (column 6, lines 20-25).

10. Claims 7, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (US Patent # 6,444,968) in view of Farrier et al. (US Patent # 6,392,260), and further in view of Applicant's admitted prior art.

11. In regard to claim 7, note the primary reference of Burt in view of Farrier discloses the use of a solid-state image sensor having a readout architecture as claimed in claim 4. Therefore, it can be seen that the Burt device lacks the use of a CCD register that includes a clearing gate and a clearing drain to remove unwanted charge. However, based on the Applicant's admission of prior art in the specification, the use of a CCD register that includes a clearing gate and a clearing drain to remove

unwanted charge is well known and expected in the art (page 11, lines 1-7; Applicant also admits that this feature is not essential to the function of the invention). Therefore, it would have been obvious to one of ordinary skill in the art to modify the primary device to include the use of a CCD register that includes a clearing gate and a clearing drain to remove unwanted charge as suggested by Applicant.

12. In regard to claim 10, note the primary reference of Burt in view of Farrier discloses the use of a solid-state image sensor having a readout architecture as claimed in claim 4. Therefore, it can be seen that the Burt device lacks the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise. However, based on the Applicant's admission of prior art in the specification, the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise is well known and expected in the art (page 4, lines 16- 20: "*However, in most CCD registers, the high field and the injection of electrons progresses along the length of the register*"). Therefore, it would have been obvious to one of ordinary skill in the art to modify the primary device to include the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise as suggested by Applicant.

13. In regard to claim 11 (numbered 12), note the primary reference of Burt in view of Farrier discloses the use of a solid-state image sensor having a readout architecture as claimed in claim 4. Therefore, it can be seen that the Burt device lacks the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise. However, based on the Applicant's admission of prior art in the specification, the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate wherein charge flows in that one direction through a high electrical field to minimize charge multiplication pulse amplitude is well known and expected in the art (page 4, lines 16- 20: "*However, in most CCD registers, the high field and the injection of electrons progresses along the length of the register*"). Therefore, it would have been obvious to one of ordinary skill in the art to modify the primary device to include the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate wherein charge flows in that one direction through a high electrical field to minimize charge multiplication pulse amplitude as suggested by Applicant.

Allowable Subject Matter

14. Claims 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. As for claims 5, the prior art does not teach or fairly suggest the use of a solid-state image sensor having a readout architecture having a CCD register having a

progressively wider width, wherein the width of the register and the number of charge multiplication elements varies according to a predetermined formula.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US005337340A: note the use of charge multiplication elements in a CCD register.

US005652442A: note the use of CCD register with a charge boundary.

US004873561: note the use of a CCD register with antiblooming structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chriss S. Yoder, III whose telephone number is (703) 305-0344. The examiner can normally be reached on M-F: 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CSY
July 22, 2004

TUAN HO
PRIMARY EXAMINER